ABSTRACT OF THE DISLCOSURE

TRACING MULTIPLE DATA ACCESS INSTRUCTIONS

A microprocessor integrated circuit 104 is provided with a trace controller 120 that is responsive to trace initiating conditions to trigger commencement of tracing operation and generation of a trace data stream. In the case of a multi-word data transfer instruction LSM, the trace controller 120 is able to trigger tracing partway through that instruction such that a subset of the transfer specified by that instruction are included within the trace data stream. All transfers subsequent to the triggering transfer may be traced with those transfers subsequent to the triggering transfer being marked with place holder codes rather than more informative full trace data for the triggering transfer.

[Figure 11]